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Design and Simulation of superconducting fault current limiter

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Abstract: *In this paper, Interruptions to supply and sags of distribution system voltage are the main aspects causing customer complaints. There is a need for analysis of supply reliability and voltage sag to relate system performance with network structure and equipment design parameters. This analysis can also give prediction of voltage dips, as well as relating traditional reliability and momentary outage measures to the properties of protection systems and to network impedances. Existing reliability analysis software often requires substantial training, lacks automated facilities, and suffers from data availability. Thus it requires time-consuming manual intervention for the study of large networks. Distribution system reliability can be divided into two aspects: system adequacy and system security. Adequacy describes the normal state capability of the system to supply customer demands. Security describes the ability of the system to continue to supply the customer in spite of faults in the network. In this paper, the improvement of the voltage sag is analyzed according to the fault location, resistance value of SFCL, and the length of the loop power distribution system. First, a resistor-type SFCL model is used using the MATLAB/SIMULINK. Next, the loop power distribution system is modeled. Finally, when the SFCL is installed in the radial or loop power distribution system with various lengths, voltage sags are evaluated according to various fault locations. The results of voltage sag analysis in the loop system are compared with the voltage sags in radial power distribution system.*
In extension to the work discussed in paper the system can be tested under different fault conditions and a study on positioning of super conducting fault current limiter can be analyzed. And also SFCL is replaced with FCL.
Index Terms: *Loop power distribution system, superconduct-ing fault current limiter (SFCL), voltage sag.*

I. Introduction

Superconducting fault current limiter is a promising technique to limit fault current in power system. Normally non-linear characteristic of superconductor is used in SFCL to limit fault current. In a normal operating condition SFCL has no influence on the system due to the virtually zero resistance below its critical current in superconductors. But when system goes to abnormal condition due to the occurrence of a fault, current exceeds the critical value of superconductors resulting in the SFCL to go resistive state. Different types of SFCLs have been developed until now. Many models for SFCL have been designed as resistor-type, reactor-type, and transformer -type etc. In this paper a resistive-type SFCL is modeled using simulink. Quench and recovery characteristics are designed on the basis of the magnitude of sag.

, whereas it may worsen the duration of sag because of the delayed trip time of a protective device by the decreased fault current. These effects of SFCL on voltage sags should be evaluated. Also, power distribution system will be changed to loop system such as microgrid or smartgrid. Thus, effects of SFCLs should be evaluated and analyzed when SFCLs are installed in radial and loop power distribution sys-tem according to the location and impedance of SFCL, the length of feeder, and location of fault. However, the overall ef-fects on voltage sag were not dealt with in the above mentioned studies.

In this paper, we assess the impact of SFCL on voltage sags in radial and loop power distribution system. In Section II, we model a resistor-type SFCL. In Section III, the voltage sag oc-curred by fault current is explained. In Section IV, we evaluate the voltage sag magnitude according to the fault location and re-sistance of SFCL in radial and loop power distribution system.

II. Modeling And Simulation

A. Resistive SFCL Model

Simulink/SimPowersystem is chose to design resistive SFCL. Four fundamental parameters is used for modeling resistive-type SFCL.
The parameters and their values are:
Transition or response time = 2ms,
minimum impedance=0.01Ω & maximum impedance= 20Ω,
triggering current=550A,
recovery time =10ms.

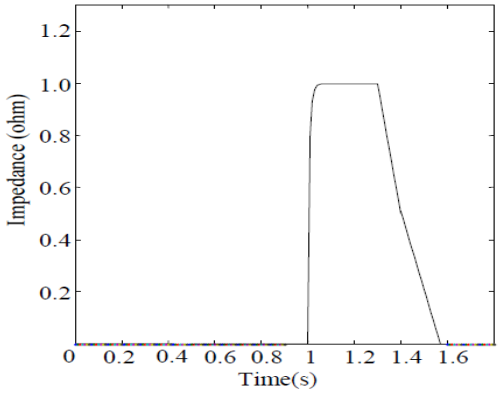


Figure 1. Quench and Recovery characteristics of SFCL

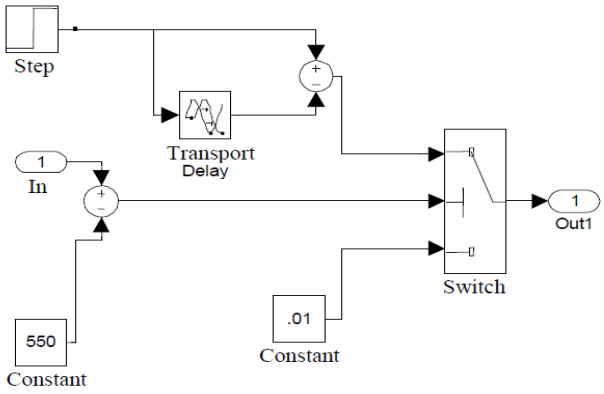


Figure 2. Implementation of resistive SFCL characteristics in Simulink

These parameters are used for implementing resistive SFCL characteristic is shown in Fig. 2. Quenching and recovery time of SFCL are specified using step and transport block respectively. A Switch block is used to give minimum or maximum impedance in output which is determined considering the incoming current. The simulation model of SFCL for a single phase system is shown in Fig.3. The working principle of the SFCL model developed in Simulink/SimPowersystem is described below. Firstly, RMS value of incoming current (passing through current measurement block) is measured by RMS block.

Then itcompares the current with the specified current in the SFCL subsystem. SFCL gives minimum resistance, if the incoming current is less than the triggering current level. But if thecurrent is larger than the triggering current, SFCL's impedance rises to maximum state. It ultimately raises thetotal impedance of the system which results in limiting thefault current. Finally, the SFCL's resistance will be minimumwhen the limited fault current is below the triggering values.

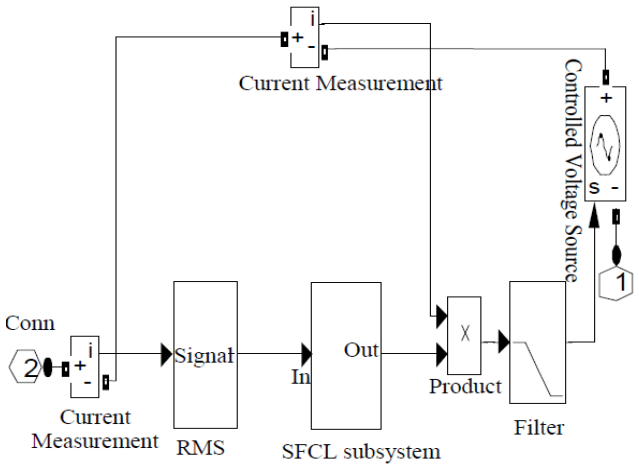


Figure 3. Resistive SFCL model in Simulink

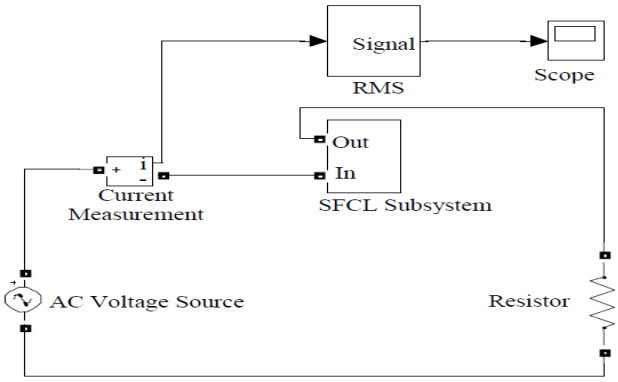


Figure 4. Simulation model of single phase system withSFCL

B. Modeling of SFCL to demonstrate Current Limiting Characteristics

The designed model of SFCL is implemented in single phase system and fault current characteristics are taken with and without SFCL. The simulation model for this purpose is shown in fig.4 and fig.5 respectively. The fault is introduced directly through AC source in order to decrease the difficulty of simulation. An RMS block is used to calculate the RMS value of the incoming current and scope is used to see the output o the sytem.

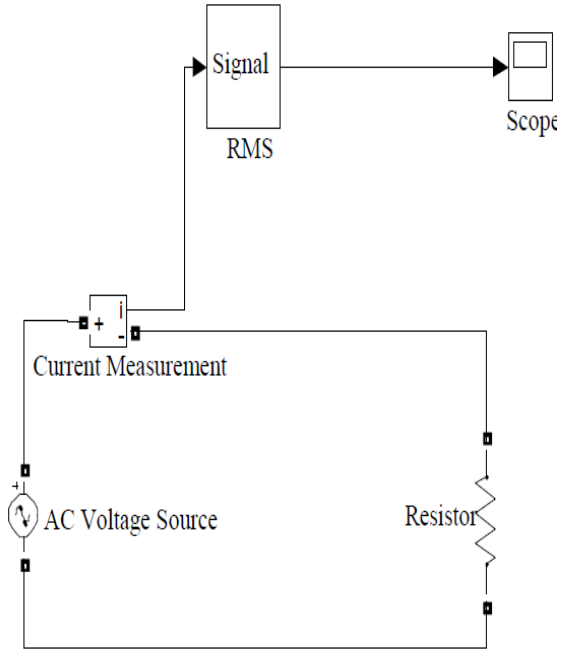


Figure 5. Simulation model of single phase system without SFCL

III. Voltage Sags In Power Distribution System

When faults occur in power distribution system, the automaticrecloser or circuit breaker with over-current relay (OCR)and reclosing relay will open to clear the fault and automatically reclose after a time delay. This reclosing behavior can take place several times in an effort to establish a continuous service when a temporary fault occurs . The voltage sag generally happens from fault.

In case 1 in Fig. 2(a), if a temporary fault occurs between CB and recloser, the reclosing operation of the OCR of breaker will be successful and the momentary interruption will occur. In this case, the customers at feeder 1 (faulted feeder) will experience a voltage sag and a momentary interruption. The customers at feeder 2 (neighbor feeder) will experience the voltage sag during the three voltage sags, two momentary interruptions and a sustained interruption. The customers in feeder 2 will experience two voltage sags during the fast-trip time of OCR and one voltage sag during the delay-trip time of OCR when reclosing scheme of OCR is 1F1D, this is shown in Fig. 6(c).during a fault. In case 2 in Fig. 6(a), all sequences and phenomena is equal to that of case 1 such as the number of voltage sags, three voltage sags, two momentary interruptions and a sustained interruption. The customers in feeder 2 will experience two voltage sags during the fast-trip time of OCR and

one voltage sag during the delay-trip time of OCR when reclosing scheme of OCR is 1F1D, this is shown in Fig. 6(c).during a fault.In case 2 in Fig. 6(a), all sequences and phenomena is equal to that of case 1 such as the number of voltage sags,momentary interruptions, and sustained interruption except the fault clearing time of recloser instead of OCR. In other words, if a temporary fault is occurs, the customers at feeder 2 will experience the voltage sag during the fast-trip time of recloser instead of OCR, so on. As presented above, the automatic reclosing scheme in power distribution systems can produce various voltage sags to the customers on the neighbor feeder. Moreover, the number of neighbor feeder is about 6 to 10 while the number of faulted feeder is only one. Also, when a fault occurs, the customers at each feeder experienced the various magnitude of voltage according to many factors such as line impedance, fault location, types of fault, and so on. Generally, a voltage magnitude at bus of secondary-side of main transformer (MTr.) during fault can be represented as equation (2) if fault impedance is ignored, a type of fault is 3-phase fault, and source voltage is 1.0 p.u.

$$V_{bus} = \frac{Z_{line}}{Z_{source} + Z_{MTr} + Z_{line}} \quad (1)$$

where Z_{source}, Z_{MTr}, and Z_{line} are source impedance, trans-former impedance, and line impedance from source to faulted location, respectively. Equation (2), also, can approximately represent the voltage magnitude at customers on all neighbor feeders. In this paper, the voltage magnitude is focused than sag duration.

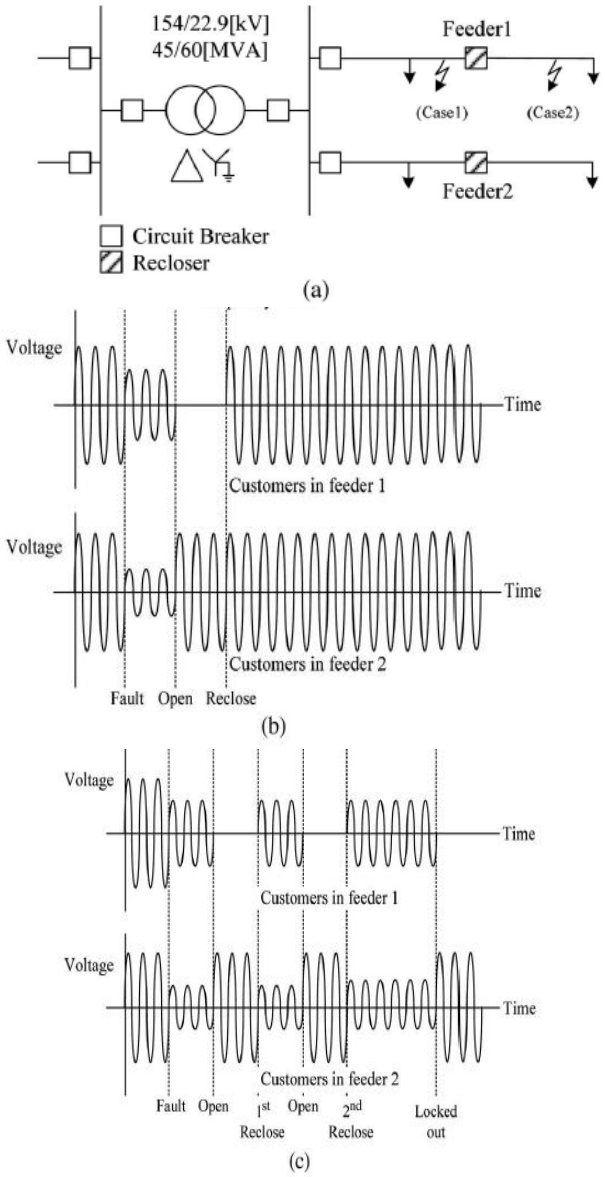


Fig. 6. Voltage sag in power distribution system d. (a) Power system configuration, (b) voltage sags of customers (temporary fault), and (c) voltage sags of customers (permanent fault

IV. Proposed FCL Configuration And Its Operation

Fig. 7 shows the circuit topology of the proposed FCL which is composed of the two following parts: Bridge part that includes a diode rectifier bridge, a small dc limiting reactor (L_{dc}) . (Note that its resistance (R_{dc}) is involved too.), a semiconductor switch (IGBT or GTO), and a free wheeling diode (D_5) Shunt branch as a compensator that consists of a resistor and an inductor $(R_{sh}+j\omega L_{sh})$.

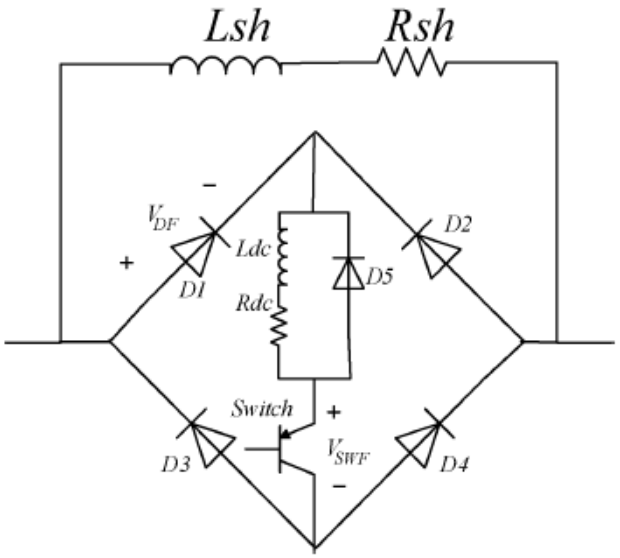


Fig. 7. Proposed FCL topology

Previously introduced structures for this application have used two numbers of thyristors at bridge branches in-stead of one semiconductor switch inside the bridge (dc current route). Therefore, first, they have the more complicated control system. Second, in those structures, because of thyristors' oper-ation delay (turn off at the first zero crossing), L_{dc} has a large value to limit the fault current between the fault occurrence in-stant and thyristors turn off instant, properly. This large value of L_{dc} leads to a considerable voltage drop on the FCL .

$$P_{loss} = P_R + P_D + P_{SW}$$
$$= R_{dc}I_{dc}^2 + 4V_{DF}I_{ave.} + V_{SWF}I_{dc} \quad (2)$$

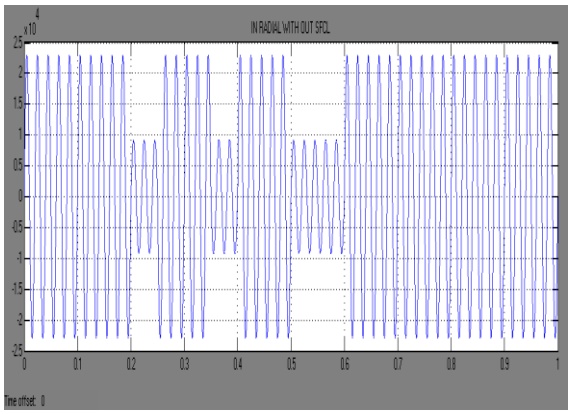
(9) and the small value of dc reactor in this structure, the total power losses of the proposed structure become a very small percentage of the feeder's transmitted power. For example, by considering Table I parameters in the simulation section, the power losses will be 0.47% of the feeder's transmitted power.

V. Case Study

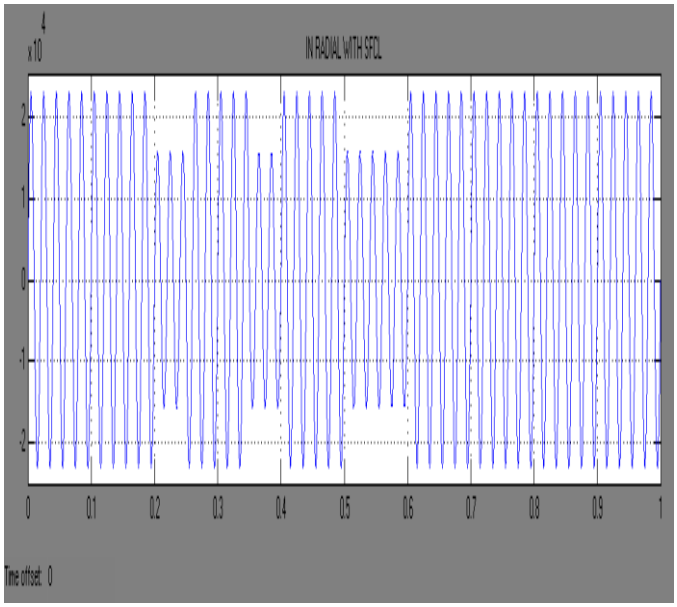
LOAD SIDE OUTPUT VOLTAGE WAVEFORMS:

1. VLOTAGE SAG IN RADIAL SYSTEM:

A.WITHOUT SFCL:

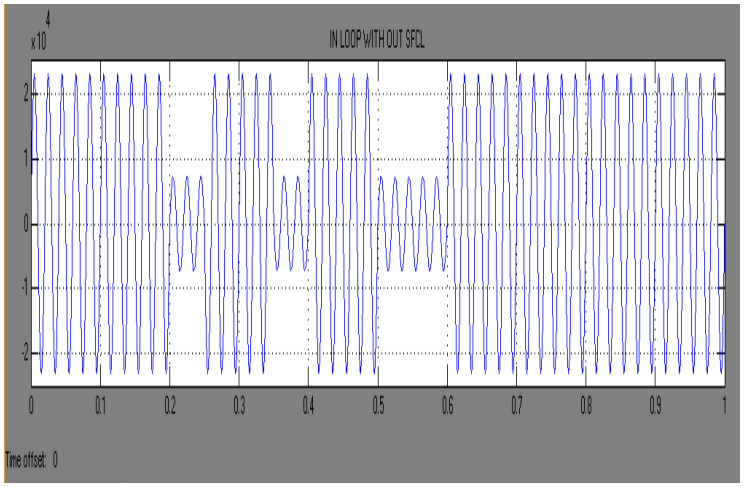


B. With SFCL:

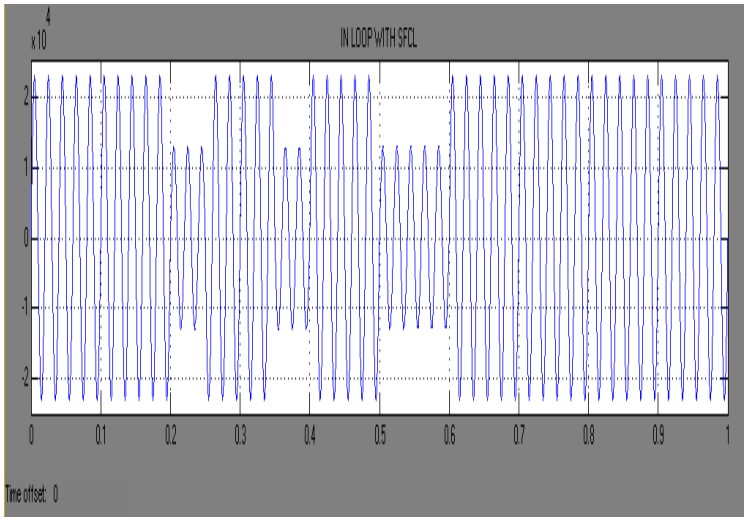


2 .IN LOOP DISTRIBUTION SYSTEM VOLTAGE SAG WAVEFORM:

A.WITHOUT SFCL

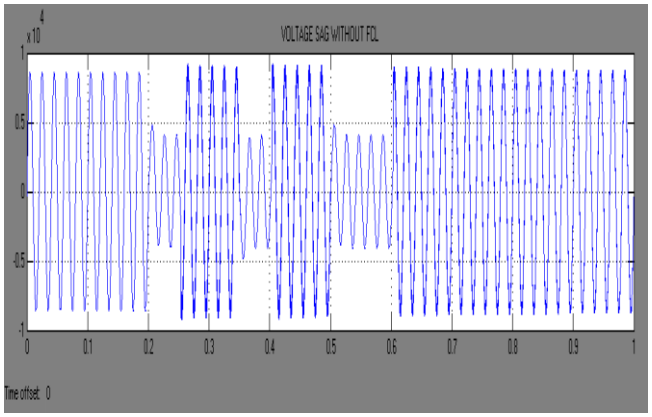


B. SFCL

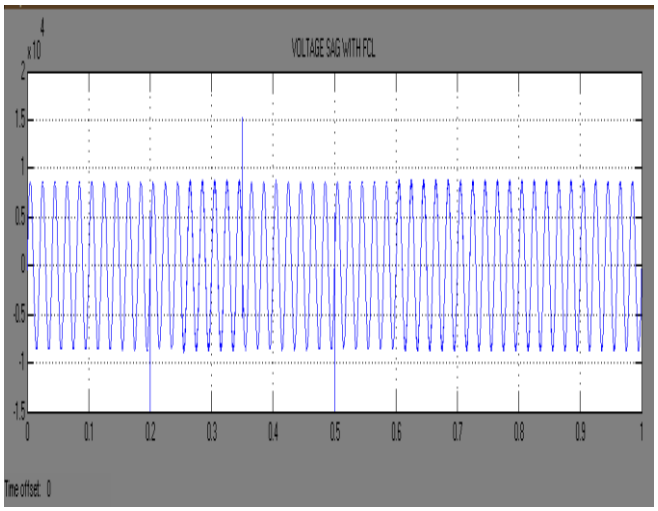


VI. Experimental Results

A. VOLTAGE SAG WITHOUT FCL:



B. VOLTAGE SAG WITH FCL:



VII. Conclusion

In this paper, the effect of FCL on voltage sag is analyzed when a FCL is installed to a radial and loop power distribution system. Firstly, resistor-type FCL and radial/loop power distribution system are modeled. Voltage magnitudes are analyzed according to fault locations and FCL's resistance values, and the lengths of loop system. The simulation results found that FCL will totally compensate the voltage sag as compared with SFCL. FCL is more efficient than SFCL in cost and compensation of sag.

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