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An Integrated Step-Down Converter Using Single-Stage Single-Switch

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ABSTRACT: *This paper presents a high step-down tranformerless single-stage single-switch ac/dc converter suitable for universal line applications (90–270 V_{rms}). The topology integrates a buck-type power-factor correction (PFC) cell with a buck–boost dc/dc cell and part of the input power is coupled to the output directly after the first power processing. With this direct power transfer feature and sharing capacitor voltages, the converter is able to achieve efficient power conversion, high power factor, low voltage stress on intermediate bus (less than 130 V) and low output voltage without a high step-down transformer. The absence of transformer reduces the component counts and cost of the converter. Unlike most of the boost-type PFC cell, the main switch of the proposed converter only handles the peak inductor current of dc/dc cell rather than the superposition of both inductor currents. Detailed analysis and design procedures of the proposed circuit are given and verified by experimental results.*

INDEX TERMS: *Direct power transfer (DPT), integrated buck– buck–boost converter (IBuBuBo), power-factor correction (PFC), single-stage (SS), transformerless*.

I. INTRODUCTION

SINGLE-STAGE (SS) ac/dc converters have received much attention in the past decades because of its cost effective-ness, compact size, and simple control mechanism. Among ex-isting SS converters, most of them are comprised of a boost power-factor correction (PFC) cell followed by a dc/dc cell for output voltage regulation [1]–[7]. Their intermediate bus voltage is usually greater than the line input voltage and easily goes be-yond 450 V at high-line application [8]. Although there are a lot of efforts to limit this bus voltage, it is still near or above the peak of the line voltage due to the nature of boost-type PFC cell. For application with low output voltage (e.g., ≤48V), this high inter-mediate bus voltage increases components stresses on the dc/dc cell. With a simple step-down dc/dc cell (i.e. buck or buck–boost converter), extremely narrow duty cycle is needed for the con-version. This leads to poor circuit efficiency and limits the input voltage range for getting better performance [9], [10]. Therefore, a high step-down transformer is usually employed even when galvanic isolation is not mandatory. For example, LED drivers without isolation may satisfy safety requirement [11]. Also, in some multistage power electronics system (e.g., in data center, electrochemical and petrochemical industries, and subway ap-plications [12]), the isolation has been done in the PFC stage, the second transformer in the dc/dc cell for the sake of isolation is considered as redundant. Hence, nonisolated ac/dc converter can be employed to reduce unnecessary or redundant isolation and enhance efficiency of the overall system. Besides, leakage inductance of the transformer causes high spike on the active switch and lower conversion efficiency. To protect the switch, snubber circuit is usually added resulting in more component counts [13]. In addition, the other drawbacks of the boost-type PFC cell are that it cannot limit the input inrush current and provide output short-circuit protection [14].To tackle the aforementioned problems, an effective way is to reduce the bus voltage much below the line input voltage. Several topologies have been reported [9], [10], [13], [15]–[18]. Although the recently reported IBoBuBo converter [13] is able to limit the bus voltage under 400 V, it cannot be applied to the low-voltage application directly due to the boost PFC cell. On the other hand, the converters [9], [10], [15]–[18] employ dif-ferent PFC cells to reduce the intermediate bus voltage. Among those converters, [9] and [15] use a transformer to achieve low output voltage either in PFC cell or dc/dc cell. Therefore, the leakage inductance is unavoidable. In [10], [17], and [18], the converters employ a buck–boost PFC cell resulting in negative polarity at the output terminal. In addition, the topologies in [18] and [10] process power at least twice resulting in low power ef-ficiency. Moreover, the reported converters, in [16], and [17], consist of two active switches leading to more complicated gate control.

Apart from reducing the intermediate bus voltage, the con-verter in [19] employs resonant technique to further increase the step-down ratio based on a buck converter to eliminate the use of intermediate storage capacitor. The converter features with zero-current switching to reduce the switching loss. However, without the intermediate storage, the converter cannot provide hold-up time and presents substantial low-frequency ripples on its output voltage. Besides, the duty cycle of the converter for high-line input application is very narrow, i.e.,

< 10%. This greatly increases the difficulty in its implementation due to the minimum on-time of pulse-width-modulation (PWM) IC and rise/fall time of MOSFET. More details on comparing different approaches will be given in the Section V. In this paper, an intergrated buck–buck–boost (IBuBuBo) converter with low output voltage is proposed. The converter utilizes a buck converter as a PFC cell. It is able to reduce the bus voltage below the line input voltage effectively. In addition, by sharing voltages between the intermediate bus and output capacitors, further reduction of the bus voltage can be achieved. Therefore, a transformer is not needed to obtain the low output voltage.

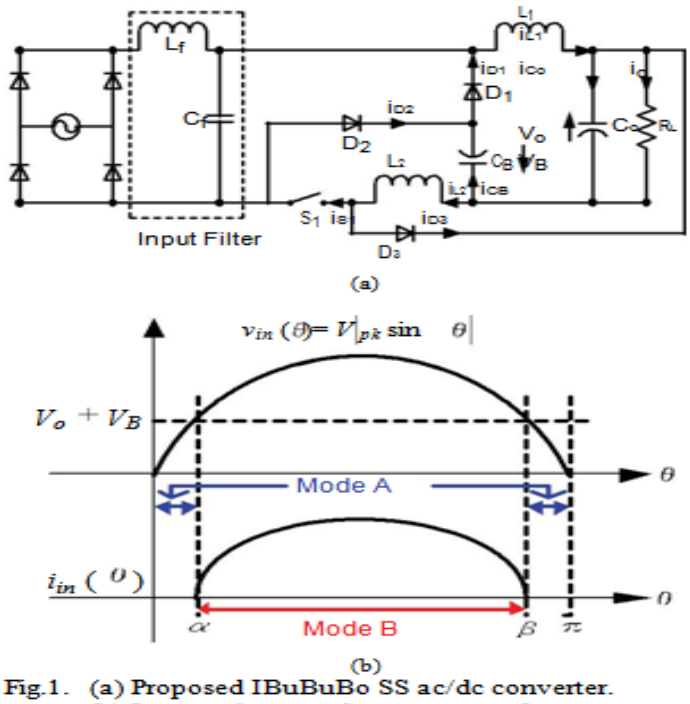


Fig.1. (a) Proposed IBuBuBo SS ac/dc converter. (b) Input voltage and current waveforms.

To sum up, the converter is able to achieve:

[1] Low intermediate bus and output voltages in the absence of transformer;
[2] Simple control structure with a single-switch;
[3] Positive output voltage;
[4] High conversion efficiency due to part of input power is processed once and
[5] Input surge current protection because of series connection of input source and switch.

The paper is organized as follows: operation principle of the proposed IBuBuBo converter is depicted in Section II and fol-lowed by design consideration with key equations in Section III. Experimental result and discussion of the converter are given in Section IV and V, respectively. Finally, conclusion is stated in Section VI.

II. PROPOSED CIRCUIT AND ITS OPERATING PRINCIPLE

The proposed IBuBuBo converter, which consists of the merging of a buck PFC cell (L_1 , S_1 , D_1 , C_o , and C_B) and a buck–boost dc/dc cell (L_2 , S_1 , D_2 , D_3 , C_o , and C_B) is il-lustrated in Fig. 1(a). Although L_2 is on the return path of the buck PFC cell, it will be shown later in Section III-A that it does not contribute to the cell electrically. Thus, L_2 is not con-sidered as in the PFC cell. Moreover, both cells are operated in discontinuous conduction mode (DCM) so there are no currents in both inductors L_1 and L_2 at the beginning of each switching cycle t_0 . Due to the characteristic of buck PFC cell, there are two operating modes in the circuit.

Mode A ($v_{in}(\theta) \leq V_B + V_o$): When the input voltage $v_{in}(\theta)$ is smaller than the sum of intermediate bus voltage V_B , and output voltage V_o , the buck PFC cell becomes inactive and does not shape the line current around zero-crossing line voltage [20], owing to the reverse biased of the bridge rectifier. Only the buck–boost dc/dc cell sustains all the output power to the load. Therefore, two dead-angle zones are present in a half-line period and no input current is drawn as shown in Fig. 1(b). The circuit operation within a switching period can be divided into three stages and the corresponding sequence is Fig. 2(a),(b), and (f). Fig. 3(a) shows its key current

waveforms.

[1] Stage 1 (period $d_1 T_s$ in Fig. 3) [see Fig. 2(a)]: When switch S_1 is turned ON, inductor L_2 is charged linearly by the bus voltage V_B while diode D_2 is conducting. Output capacitor C_o delivers power to the load.

[2] Stage 2 (period $d_2 T_s$ in Fig. 3) [see Fig. 2(b)]: When switch S_1 is switched OFF, diode D_3 becomes forward biased and energy stored in L_2 is released to C_o and the load.

[3] Stage 3 (period $d_3 T_s$ - $d_4 T_s$ in Fig. 3) [see Fig. 2(f)]: The inductor current $i_{L\ 2}$ is totally discharged and only C_o

[4] sustains the load current.

Mode B ($v_{in}(\theta) > V_B + V_o$): This mode occurs when the input voltage is greater than the sum of the bus voltage and output voltage. The circuit operation over a switching period can be divided into four stages and the corresponding sequence is Fig. 2(c), (d), (e), and (f). The key waveforms are shown in Fig. 3(b).

[1] Stage 1 (period $d_1 T_s$ in Fig. 3) [see Fig. 2(c)]: When switch S_1 is turned ON, both inductors L_1 and L_2 are charged linearly by the input voltage minus the sum of the bus voltage and output voltage ($v_{in}(\theta) - V_B - V_o$), while diode D_2 is conducting.

[2] Stage 2 (period $d_2 T_s$ in Fig. 3) [see Fig. 2(d)]: When switch S_1 is switched OFF, inductor current $i_{L\ 1}$ decreases linearly to charge C_B and C_o through diode D_1 as well as transferring part of the input power to the load directly. Meanwhile, the energy stored in L_2 is released to C_o and the current is supplied to the load through diode D_3 . This stage ends once inductor L_2 is fully discharged.

[3] Stage 3 (period $d_3 T_s$ in Fig. 3) [see Fig. 2(e)]: Inductor L_1 continues to deliver current to C_o and the load until its current reaches zero.

[4] Stage 4 (period $d_4 T_s$ in Fig. 3) [see Fig. 2(f)]: Only C_o delivers all the output power.

III. DESIGN CONSIDERATIONS

To simplify the circuit analysis, some assumptions are made as follows:

1) All components are ideal;
2) Line input source is pure sinusoidal, i.e. $v_{in}(\theta) = V_{pk}\ sin(\theta)$ where V_{pk} and θ are denoted as its peak voltage and phase angle, respectively;

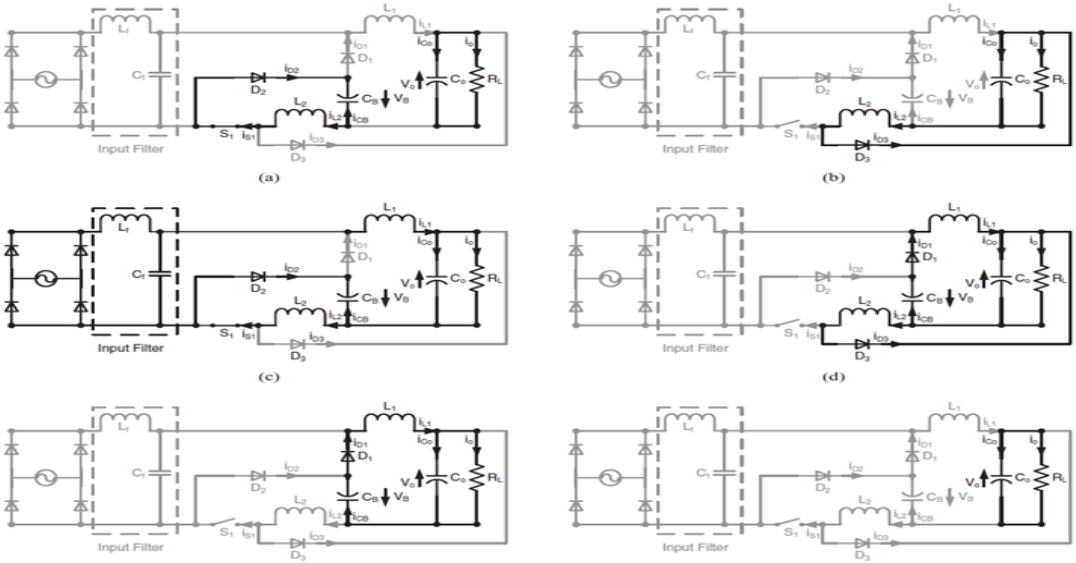


Fig. 2. Circuit operation stages of the proposed ac/dc converter.

3) Both capacitors C_B and C_o are sufficiently large such that they can be treated as constant DC voltage sources without any ripples;
4) The switching frequency f_s is much higher than the line frequency such that the rectified line input voltage $|v_{in}(\theta)|$ is constant within a switching period.

A. Circuit Characteristics

According to Fig. 1(b), there is no input current drawn from the source in Mode A, and the phase angles of the dead-time α and β can be expressed as

$$\alpha = arcsin\left(\frac{V_T}{V_{pk}}\right)$$

$$\beta = \pi - \alpha = \pi - arcsin\left(\frac{V_T}{V_{pk}}\right). \qquad (1)$$

where V_T is the sum of V_B and V_o. Thus, the conduction angle of the converter is

$$\gamma = \beta - \alpha = \pi - 2arcsin\left(\frac{V_T}{V_{pk}}\right). \qquad (2)$$

From the key waveforms (see Fig. 3), the peak currents of the two inductors are

$$i_{L1\_pk} = \begin{cases} \frac{v_{in}(\theta)-V_T}{L_1} d_1 T_s, & \alpha<\theta<\beta \\ 0, & otherwise \end{cases} \qquad (3)$$

and

$$i_{L1\_pk} = \frac{V_B}{L_2} d_1 T_s \qquad (4)$$

where T_s ($1/f_s$) is a switching period of the converter. In (3) and (4), the dependency of i_{L1_pk} on θ has been omitted for clarity. It is noted $L2$ does not contribute in (3) even though it is on the current return path of the PFC cell.

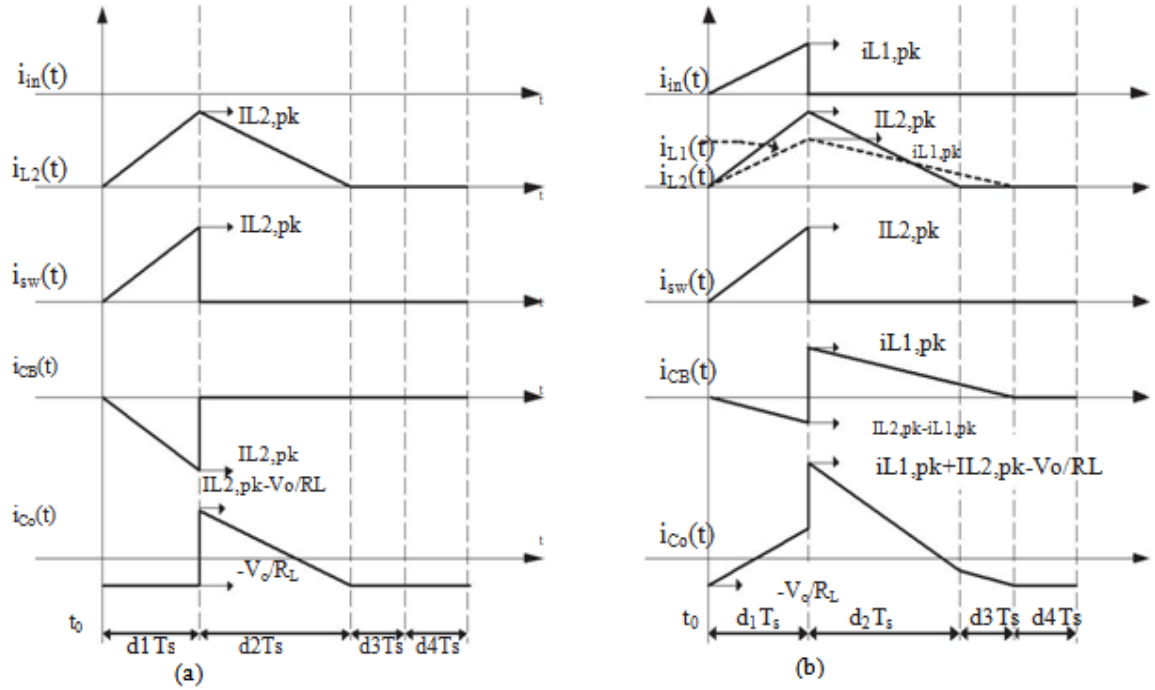


Fig. 3.key waveforms of the proposed circuit

In addition, by considering volt–second balance of the L_1 and L_2, respectively, the important duty ratio relationships can be expressed as follows:

$$d_2 + d_3 = \begin{cases} \frac{v_{in}(\theta)-V_T}{L_1} d_1 T_s, & \alpha<\theta<\beta \\ 0, & otherwise \end{cases} \qquad (5)$$

$$d_2 = \frac{V_B}{V_0} d_1 \qquad (6)$$

By applying charge balance of CB over a half-line period,the bus voltage V_B can be determined. From Fig. 3, the average
Current of CB over a switching and half-line periods are expressed as follows:

$$< i_{CB} >_{sw} = \frac{1}{2}\left(i_{L1_{pk}}(d_1 + d_2 + d_3) - i_{L2_{pk}} d_1\right)$$

$$= \frac{d_1^2 T_s}{2}\left[\frac{(v_{\text{in}}(\theta)\text{-}V_T)v_{\text{in}}(\theta)}{L_1 V_T} - \frac{V_B}{L_2}\right] \qquad (7)$$

and

$$< i_{CB} >_{\pi} = \frac{1}{\pi}\int_0^{\pi} < i_{CB} >_{sw} d\theta$$

$$= \frac{d_1^2 T_s}{2\pi}\left[\frac{V_{pk}}{L_1}\left(V_{pk} V_t\left(\frac{\gamma}{2} + \frac{A}{4}\right) - B\right) - \frac{\pi V_B}{L_2}\right] \qquad (8)$$

where the constants A and B are

$$A = \sin(2\alpha) - \sin(2\beta) \qquad (9)$$

$$B = \cos(\alpha) - \cos(\beta) \qquad (10)$$

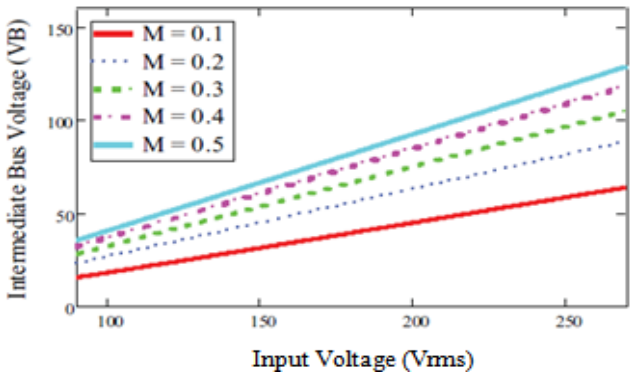


Fig. 4. Calculated intermediate bus voltage under different inductance ratios.

$$V_B = \frac{MV_{pk}^2}{2\pi(V_B + V_o)} \times \left[\pi - 2arcsin\left(\frac{V_B + V_o}{V_{pk}}\right) - \frac{2(V_B + V_o)\sqrt{(V_{pk} + V_b + V_o)(V_{pk} + V_B + V_o)}}{V_{pk}^2}\right] \qquad (11)$$

where M is the inductance ratio $L2/L1$.

As observed from (11), the bus voltage VB can be obtained easily by numerical method. It is noted that VB is independent on the load, but dependent on the inductance ratio M. Fig. 4 depicts the relationship among VB , rms value of the line voltage, and inductance ratio M. It is noted that the bus voltage is kept below 150 V at high-line input condition.

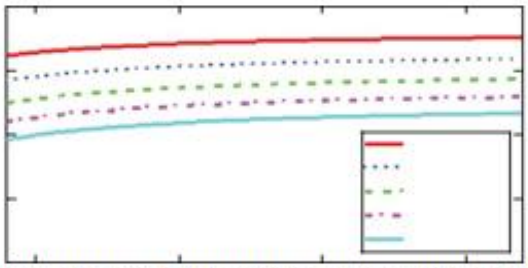


Fig. 5. Estimated Power Factor under variation of inductance ratios.

Input Voltage (Vrms)

Similarly, the instantaneous and average input currents of the proposed circuit are

$$< \mathrm{i_{in}} >_{sw} = \frac{i_{L1\_pk}\, d_1}{2} = \begin{cases} \frac{v_{in}(\theta)\text{-}V_T}{2L_1} d_1^2 T_s, & \alpha<\theta<\beta \\ 0, & otherwise \end{cases} \quad (12)$$

and

$$I_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} < \mathrm{i_{in}} >_{sw} d\theta$$

$$= \frac{d_1^2 T_s}{2\pi L_1}[V_{PK}B - \gamma V_T] \quad (13)$$

Using (12) and (13), the rms value of the input current, average input power and power factor are given by

$$I_{in\_rms} = \sqrt{\frac{1}{\pi}\int_{\alpha}^{\beta}(< \mathrm{i_{in}} >_{sw})^2 d\theta}$$

$$= \frac{d_1^2 T_s}{2\sqrt{\pi} L_1}\sqrt{V_{pk}^2\left(\frac{\gamma}{2}+\frac{A}{4}\right) - 2V_{PK}V_T B + \gamma {V_T}^2}; \quad (14)$$

$$P_{in} = \frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) < \mathrm{i_{in}} >_{sw} d\theta$$

$$= \frac{d_1^2 T_s V_{PK}}{2\pi L_1}\left[V_{pk}\left(\frac{\gamma}{2}+\frac{A}{4}\right) - V_T B\right] \quad (15)$$

$$\mathrm{PF} = \frac{\frac{1}{\pi}\int_{\alpha}^{\beta} v_{in}(\theta) <\mathrm{i_{in}} >_{sw} d\theta}{\frac{V_{pk}}{\sqrt{2}} I_{in\,rms}}$$

$$= \sqrt{\frac{2}{\pi}}\frac{V_{pk}\left(\frac{\gamma}{2}+\frac{A}{4}\right) - V_T B}{\sqrt{V_{pk}^2\left(\frac{\gamma}{2}+\frac{A}{4}\right) - 2V_{PK}V_T B + \gamma {V_T}^2}} \quad (16)$$

Fig. 5 exhibits the variation of power factor as a function of line input voltage and the inductance ratio M of the converter.

B. Condition for DCM

To ensure both cells working inDCMmode throughout the ac line period, we must determine their critical inductance first. To allow $L1$ working in DCM and from (5), we have the following inequalities:

$$d_2 + d_3 \le 1 - d_{1\_PFC} \quad (17)$$

and

$$d_{1\_PFC} \leq f(x) = \begin{cases} \frac{V_T}{v_{in}(\theta)}, & \alpha < \theta < \beta \\ 0, & otherwise \end{cases} \quad (18)$$

where $d1$ PFC is the maximum $d1$ of the PFC cell. For the buck–boost dc/dc cell working in DCM mode, the following inequality must be held:

$$d_2 \leq 1 - d_{1\_DC/DC} \quad (19)$$

From (6) and (19), the maximum $d1$ of the dc/dc cell is

$$d_{1\_DC/DC} \leq \frac{V_o}{V_o + V_B} = \frac{V_o}{V_T}. \quad (20)$$

Due to sharing switch in both cells of the converter, the maximum duty cycle $d1$ max of the proposed converter is

$$d_{1\_max} = \begin{cases} min(d_{1\_PFC}, d_{1\_DC/DC}), & \alpha < \theta < \beta \\ d_{1\_DC/DC}, & otherwise \end{cases} \quad (21)$$

By applying input–output power balance of the PFC cell and substituting (21) into (15), the critical inductance$L1$ crit is given by

$$L_{1\_\text{crit}} = \frac{R_{L\_min}\, T_s\, V_{PK} V_T}{2\pi V_0^2}\left[V_{PK}\left(\frac{\gamma}{2} + \frac{\sin(2\alpha)+\sin(2\beta)}{4}\right) + \left(V_T(\cos(\beta) - \cos(\alpha))\right] d_{1\_max}^2 \quad (22)$$

Where *RL* min is denoted as the minimum load resistance of the converter. For the dc/dc cell sustaining all the power to the load under DCM operation in Mode A, the critical inductance *L*2 crit is the smallest. Under the input–output power balance of the dc/dc cell, the critical inductance *L*2 crit can be determined. The input power of the dc/dc cell in Mode A is given by

$$P_{\text{in}_{\frac{DC}{DC}}} = \frac{V_B}{\pi}\int_0^{\pi} < i_{\frac{DC}{DC}} >_{sw} \, d\theta = \frac{V_B^2 T_s}{2L_2} d_1^2 \quad (23)$$

where < *idc/dc* >*sw* is the instantaneous input current of dc/dc cell.

Hence, by substituting (21) into (23), the critical inductance *L*2 crit is given by

$$L_{2\_\text{crit}} = \frac{R_{L\_min}\, V_B^2 T_s}{2V_0^2} d_{1\_max}^2 \quad (24)$$

C. Components Stresses:

Before embarking on calculating stresses on the devices, there are two characteristics of the circuit to be clarified. Interestingly, the current passing through the diode *D*2 is the difference of current between *iL*2 and *iL*1 at the time interval *d*1*Ts*. Both inductor currents flows into the diode at the interval, but in opposite direction. In addition, unlike the boost-type single-stage ac/dc converter, the current of the switch *S*1 is *iL*2, but not the superposition current of both inductors. Thus, the simultaneous currents of the diode *D*2 and switch *S*1 at interval *d*1*Ts* are

$$i_{D2} = i_{L2} - i_{L1} \quad (25)$$

$$i_{S1} = i_{L2}. \quad (26)$$

The rms current stresses on the diodes and switch are determined by averaging their rms current in a switching cycle over a half-line period. The rms current stress on the diode *D*1 over a switching cycle is

$$I_{D_1,sw\_rms} = \frac{T_s}{L_1}\sqrt{\frac{d_1^3 (v_{in}(\theta) - 2V_T)^3}{3V_T}} \quad (27)$$

Then, by taking the average of (27) over a half-line period ,its rms current stress is obtained as (28), shown in below, where $C = \cos(3\alpha) - \cos(3\beta)$.

$$I_{D_1,hf_{rms}} = \frac{T_s}{3V_T L_1}\sqrt{\frac{d_1^3}{\pi}\left[-\gamma V_T\left(8V_T^2 + 3V_{pk}^2\right) + 3V_{pk} B\left(\frac{V_{pk}^2}{4} + 4V_T^2\right) - \frac{3V_T V_{pk}^2 A}{2} - \frac{V_{pk}^3 C}{12}\right]} \quad (28)$$

Similarly, the current stresses on the other semiconductor devices can be calculated easily as

$$I_{D_2,hf\_rms} = \frac{T_s}{L_2}\sqrt{\frac{d_1^3}{3\pi}[2\alpha V_B^2 + E]} \qquad (29)$$

$$I_{D_3,hf\_rms} = \frac{V_B T_s}{L_2}\sqrt{\frac{d_1{}^3(V_B - V_0)^3}{3}} \qquad (30)$$

$$I_{S_1,hf\_rms} = \frac{V_B T_s}{L_2}\sqrt{\frac{d_1{}^3}{3}} \qquad (31)$$

$$E = \frac{1}{L_1^2}\left[\gamma(V_B L_T + L_2 V_0)^2 - 2L_2 V_{pk} B(V_B(L_1 + L_2) + L_2 V_0) + \frac{L_2^2 V_{pk}^2}{2}\left(\gamma + \frac{A}{2}\right)\right].$$

In addition, the voltage stresses on the semiconductor devices are stated in Table I.

TABLE I VOLTAGE STRESSES ON THE SEMICONDUCTOR DEVICES

Semiconductor devices	Peak Voltage
Diode D_1	V_{pk}
Diode D_2	V_{pk}
Diode D_3	V_T
Switch S_1	$V_{pk} + V_T$

D. Capacitors Optimization:

To determine the size of the intermediate bus capacitor *CB,* we can consider the hold-up time (*t*hold up) of the circuit. The bus capacitor *CB* will sustain all the output power within *t*hold up when the ac input source is removed. In normal practice, the hold-up time is one of the ac line cycle. In addition, the maximum capacitance of *CB* to meet this hold-up time requirement is determined under the low-line and full output load conditions. Thus, the size of *CB* is expressed as follows:

$$C_B = \frac{2P_0 t_{hold\_up}}{(V_B@90V_{rms})^2}. \qquad (32)$$

Apart from the size of *CB* , it is noted that the line frequency ripple on the output capacitor *Co* is inevitable since a portion of the input power is coupled to the load directly. However, this ripple can be reduced by increasing its capacitance.

E. Distribution of Direct Power Transfer:

The interaction of power processing between both PFC and dc/dc cells under low and high-line conditions is described as

$$p_0(\theta) = p_{0\_PFC}(\theta) + p_{0\_DC/DC}(\theta) \quad (33)$$

where *po* (*θ*), *po* PFC(*θ*), and *po* DC/DC(*θ*) are denoted as instantaneous output power of the converter, output power of PFC cell and output power of dc/dc cell, respectively. Both instantaneous output powers of PFC and dc/dc cells can be calculated as

$$p_{0\_PFC}(\theta) = V_0\langle i_{L1}(\theta)\rangle_{sw}$$

$$= \begin{cases} \frac{(d_1(\theta))^2 V_0 T_s}{2}\left[\frac{v_{in}(\theta)(v_{in}(\theta) - V_T)}{L_1 V_T}\right], & \alpha < \theta < \beta \\ 0, & otherwise \end{cases} \qquad (34)$$

$$p_{0\_DC/DC}(\theta) = p_{in\_DC/DC}(\theta) = V_B < i_{DC/DC} >_{sw}$$

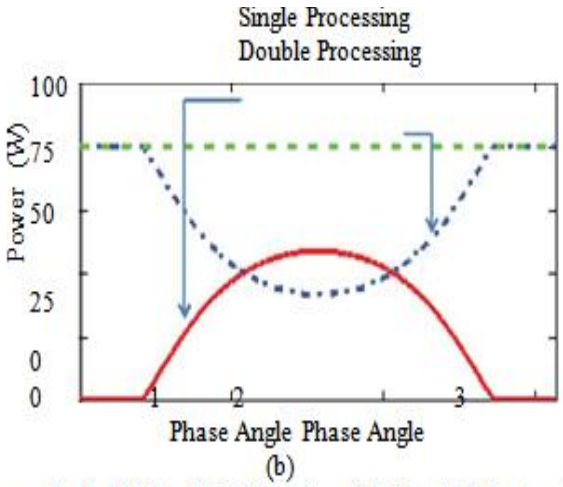
$$= \frac{V_B{}^2 T_S}{2L_2}(d_1(\theta))^2 \qquad (35)$$

where *p*in dc/dc(θ) and *d*1 (θ) are defined as the instantaneous value of input power of the dc/dc cell and duty cycle *d*1 .

From (34) and (35), it can be seen that *d*1 (θ) plays a crucial role in this analysis. *d*1 (θ) can be obtained easily once the average output current of the converter is determined. By considering the average currents of *iL*1 and *id*3 over a switching cycle, the average output current of the converter is given by

$$I_o = \begin{cases} \langle i_{L1}(\theta)\rangle_{sw} + \langle i_{d3}(\theta)\rangle_{sw}, & \alpha < \theta < \beta \\ \langle i_{d3}(\theta)\rangle_{sw}, & otherwise \end{cases}$$

$$= \begin{cases} \frac{(d_1(\theta))^2 T_s}{2}\left[\frac{v_{in}(\theta)(v_{in}(\theta)-V_T)}{L_1 V_T} + \frac{V_B^2}{L_2 V_0}\right], & \alpha < \theta < \beta \\ \frac{(d_1(\theta))^2 T_s V_B^2}{2L_2 V_0}, & otherwise. \end{cases} \quad (36)$$



(b)

Fig. 6. Calculated power processing by PFC cell (red trace) and dc/dc cell (blue trace). Condition: $P_o = 100\ W$ (green trace), $V_o = 19\ V$ and $M = 0.4$.

Hence, *d*1 (θ) in a half-line period is expressed as

$$d_1(\theta) = \begin{cases} \sqrt{\frac{2P_0}{V_0 T_s\left[\frac{v_{in}(\theta)(v_{in}(\theta)-V_T)}{L_1 V_T} + \frac{V_B^2}{L_2 V_0}\right]}}, & \alpha < \theta < \beta \\ \sqrt{\frac{2L_2 P_0}{V_B^2 T_s}}, & otherwise. \end{cases} \quad (37)$$

By substituting (37) into (34) and (35), the simultaneous output power of the converter and power distribution of the PFC and dc/dc cells are plotted as in Fig. 6. The traces of single and double power processing represent the power proceed by PFC cell *po* PFC(θ) and dc/dc cell *po* dc/dc(θ), respectively. Besides, the green dash trace is the output power (*po* total(θ)) of the converter. It is noted that the power handled by both cells is changed oppositely to maintain the load power under different input voltages. At low-line condition, there is more input power coupled to the output directly. In contrast, more power is delivered to the output by the dc/dc cell at high-line condition. More discussion of the direct power transfer is given in Section V.

III. EXPERIMENTAL RESULTS:

The performance of the proposed circuit is verified by the prototype. To ensure the converter working properly with constant output voltage, a simple voltage mode control is employed. To achieve high performance of the converter for universal line operation in terms of low bus voltage (< 150V) and high power factor (> 96%), the inductance ratio has to be optimized according to Figs. 4 and 5. The lower the bus voltage of the converter, the lower voltage rating capacitor (150 V) can be used.

TABLE II CIRCUIT COMPONENTS

Parameters	Values
IC Controller	TL594
Input filter inductor L_f	2 mH
Input filter capacitor C_f	2μF
Inductor L_1	106μH
Inductor L_2	46μH
Inductance Ratio (M = L_2/L_1)	0.434
MOSFET S_1	SPW47N60CFD
D_1	MUR3040PT
D_2	MUR3040PT
D_3	MUR3040PT
C_B	5 mF
C_o	5 mF

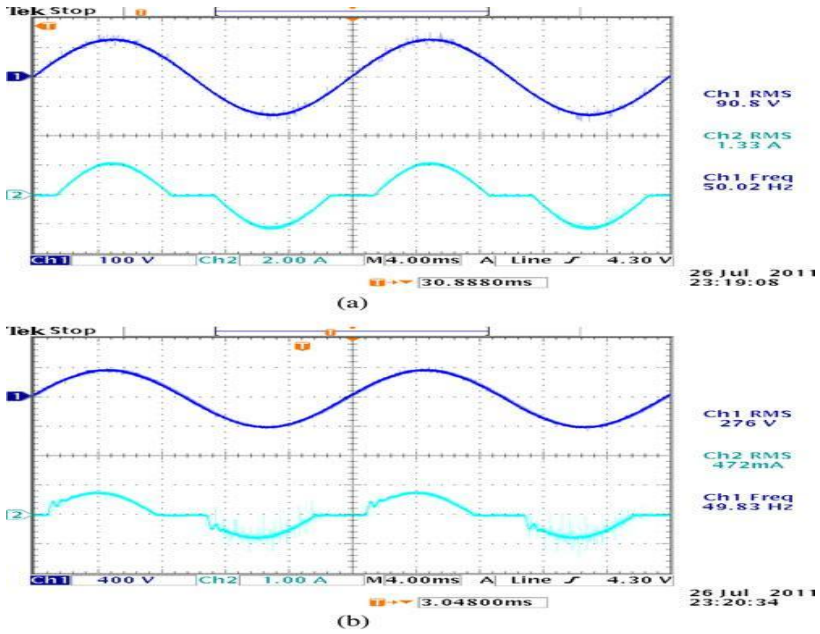


Fig. 7. Measured input characteristic of the converter at (a) 90 V_{rms} and (b) 270 V_{rms} under 100-W condition.

In addition, the inductance ratio will affect the efficiency of the converter. More detail will be given in Section V. Taking the performance of the converter on bus voltage, power factor, and efficiency into account, the inductance ratio around M = 0.4 is selected. Table II depicts all the components used in the circuit, and its specification is stated as follows:

1) Output power: 100 W;
2) Output voltage: 19 Vdc;
3) Power factor: > 96%;
4) Intermediate bus voltage: < 150V;
5) Line input voltage: 90–270 Vrms/50 Hz;
6) Switching frequency (*fs*): 20 kHz.

Current harmonics measured at 270Vrms and 100W Output

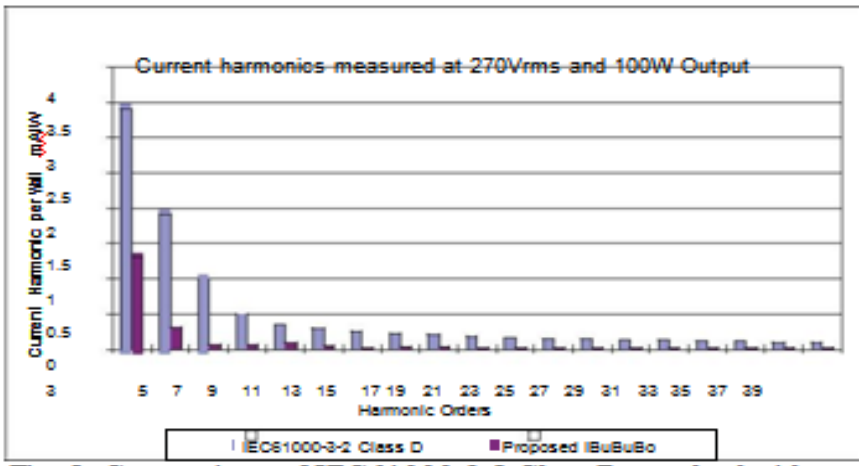


Fig. 8. Comparison of IEC61000-3-2 Class D standard with measured input current harmonics at 270 V_{rms}.

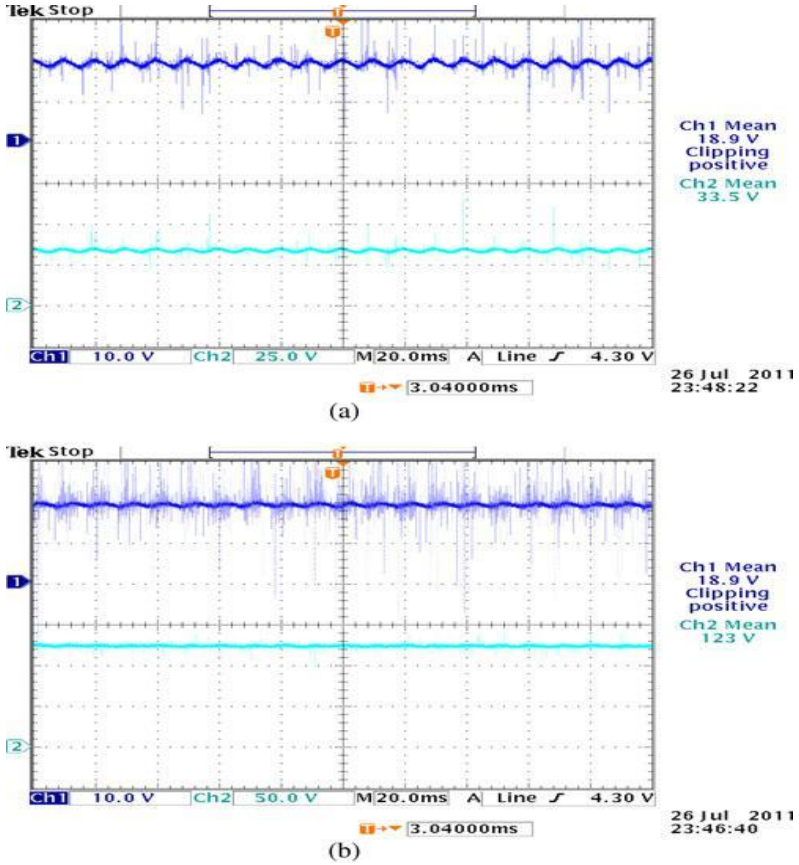


Fig. 9. Measured output voltage (upper trace −10 V/div) and intermediate bus voltage (bottom trace −40 V/div) at (a) 90 V_{rms} and (b) 270 V_{rms} under full load condition.

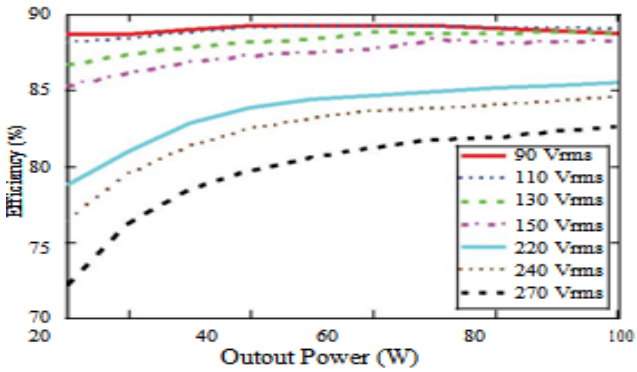


Fig. 10. Measured circuit efficiency under load variation.

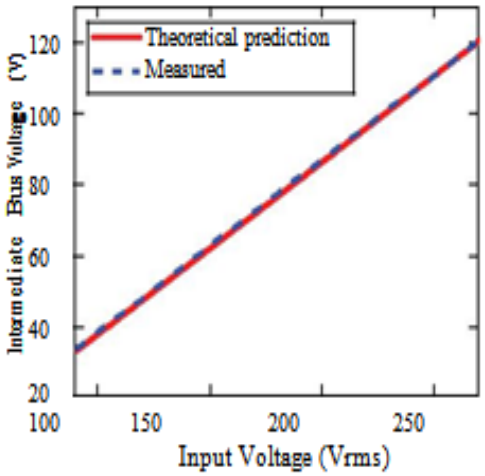


Fig. 11. Comparison of measured intermediate bus voltage with its predicted value.

The IEC61000-3-2 class D standard as shown in Fig. 8. In ad-dition, the measured output and bus voltages under both low and high line conditions are shown as in Fig. 9. It can be seen that the bus voltage was kept at 123 V and well below 150 V at high-line condition. Fig. 10 illustrates the conversion efficiency of the proposed converter under different line input and out-put power conditions. The maximum efficiency of the circuit is around 89% at low line application. Furthermore, Fig. 11 shows the predicted intermediate bus voltage is in good agreement with the measured value.

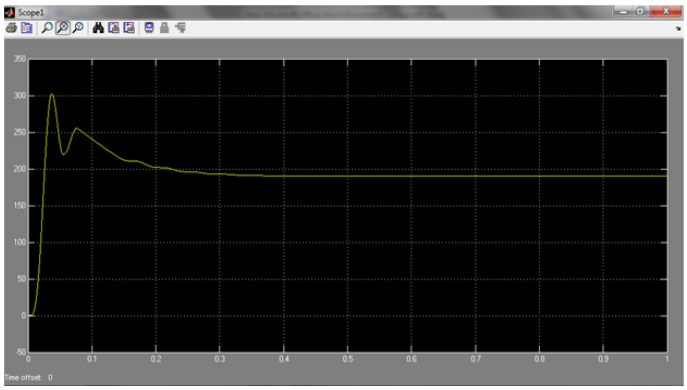


Fig: Output voltage 190 volts for R-Load Vi=390V

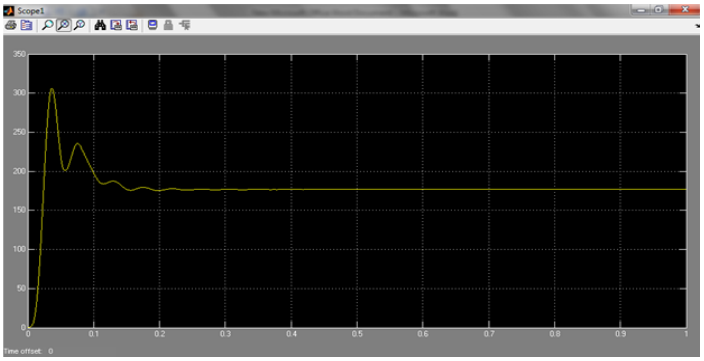


Fig: Output voltage 190 volts for Separately excited DC motor -Load Vi=390V

V. CONCLUSION

The proposed IBuBuBo single-stage ac/dc converter has been experimentally verified, and the results have shown good agree-ments with the predicted values. The intermediate bus voltage of the circuit is able to keep below 150 V at all input and output con-ditions, and is lower than that of the most reported converters. Thus, the lower voltage rating of capacitor can be used. More-over, the topology is able to obtain low output voltage without high step-down transformer. Owing to the absence of trans-former, the demagnetizing circuit, the associated circuit dealing with leakage inductance, and the cost of the proposed circuit are reduced compared with the isolated counterparts. In addition, the proposed converter can meet IEC 61000-3-2 standard, and provide both input surge current and output short-circuit protec-tion. Thanks to the direct power transfer path in the proposed converter, it is able to achieve high efficiency around 89%.

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